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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,032	02/11/2004	Sadeg M. Faris		2193

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REVEO, INC.
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ELMSFORD, NY 10523

EXAMINER	
PEACE, RHONDA S	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,032	FARIS, SADEG M.	
	Examiner	Art Unit	
	Rhonda S. Peace	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to ~~communication(s)~~ application filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-7, 9, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al (US Patent 6,444,976).

Concerning claims 1, 3-7, 9, 11, and 12, Ishikawa et al in US Patent 6,444,976 shows an optical routing switch array in two and three dimensions, comprising microspheres embedded within the substrate, indicated by the dashed-line rectangular shape on Figure 15, at each node (Figures 7 and 15, column 4 lines 26-39, column 6 lines 48-53). The microspheres are spherical active optical elements incorporating a mirror that route optical signals within the array (Figure 4, column 3 lines 66-67 and column 4 lines 1-6). In addition, these microspheres are capable of receiving and/or routing light in each of the x, y, or z-axes, in either of the positive or negative directions (Figure 15). Furthermore, Ishikawa et al describes that adding a grating to selected switches may alter the microspheres, allowing the microsphere to detect the signal. Selectively grating any of the microspheres will allow the user to predetermine the route in which they wish the optical signal to travel through the substrate (column 5 lines 11-17, Figure 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 8, 10, and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al (US Patent 6,444,976).

With reference to claims 2 and 10, the substrate indicated, as stated above, receives optical input signals from various areas outside the substrate, as shown in figure 15. This would indicate that the substrate must be transparent, to allow the said optical input signals to be properly received by the microspheres located at every node within the array. Furthermore, if the substrate is transparent, as claimed in claim 2, it is apparent that this same substrate must also be transparent to at least one wavelength of light within the spectrum, as claimed in claim 10, as no finite length of light has been specifically chosen by the applicant in claim 10.

In regards to claim 8, the substrate indicated, as mentioned above, in Figure 15 of US Patent 6,444,976 implies a multi-layer construction, since the nodes of the array are correspondingly arranged in a multi-layer fashion. Therefore, it would be obvious to one of ordinary skill in the art to incorporate a multi-layer substrate within the array, as this multi-layer design will allow for the microspheres to be activated with a greater

degree of accuracy, as each layer could be activated separately, further making the device more adaptable to industrial configurations and increasing its applicable functionality.

Concerning claims 13-15, Ishikawa et al shows the device as described above. In addition, Ishikawa et al shows this device may incorporate an integrated circuit, accessible by an optical path between the output of the circuit and the input of the array via a microsphere (column 2 lines 9-24). This would suggest that one of ordinary skill in the art is capable of incorporating any optical device previously known to be compatible with an integrated circuit into such an array as described by Ishikawa et al. Therefore, the addition of an optical device to the array as claimed by the applicant would be obvious to one of ordinary skill in the art. The addition of an optical device to the array increases the different uses of the device in various applications, further making the device more multi-functional and increasing its marketability. Furthermore, one of ordinary skill in the art would recognize that this array, along with any optical device coupled to it, would need to be stabilized in a reliable manner. One common solution to this situation is to place the optical device desired at least partially within the substrate. Therefore, having the optical device at least partially embedded within the substrate would have been obvious to one of ordinary skill in the art, as it lends the stability needed to ensure proper operation of the optical device with the array, and also increases the functional reliability of the array as its components are less susceptible to damage.

In reference to claim 16 and 17, Ishikawa et al shows the device as described

above. A common method of forming a substrate around optical elements, such as microspheres, is to place the microsphere array within a mold and pour a suitable material into the mold. With this process, it is apparent that these microspheres are not only held together by an adhesive, but also that they reside within cavities within the array. Therefore, it would have been obvious to one of ordinary skill in the art to either place the microspheres within cavities in the array, or to use an adhesive to bond the microspheres together, as these are accepted methods of substrate construction that lend stability to the array, ensuring the microspheres are well protected. In addition, this method is seen as a common and inexpensive method of forming a substrate, further reducing the cost of device's construction.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pender (US Prepublication document US 2004/0028357) describes a three-dimensional optical matrix photonic logic device that utilizes optical elements at the nodes of the array to route optical signals through the device. These optical elements may take on a number of geometries, including a spherical reflective structure, and are placed within a substrate and cladding area with the same geometrical freedom. The device as described by Pender also includes several input and output areas through which optical signals can be routed to a number of various optical devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda S. Peace whose telephone number is (571) 272-8580. The examiner can normally be reached on M-F (8-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272- 2344.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/24/05

Rhonda S. Peace
Examiner
Art Unit: 2874

John D. Lee
Primary Examiner